Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A multi-processor system comprising:

a slave processor;

a first transmission path connected to said slave processor;

a master processor connected to said first transmission path through which said master processor starts to communicate with said slave processor; and

a second transmission path which connects said slave processor and said master processor,

wherein ~~and whose~~ the transmission speed of said second transmission path is ~~smaller~~ less than ~~that~~ the transmission speed of said first transmission ~~path;~~path, and

wherein said slave processor is equipped with a command transmission means for sending a transmission request command which requests either data transmission or data reception to said master processor via said second transmission path; and

said master processor is equipped with a data transmission means for starting data transmission to said slave processor via said first transmission path in response to said transmission request command.

2. (currently amended): A multi-processor system comprising:

a slave processor, which is defined ~~(defined~~ as a slave relative to a master ~~processor)~~processor, the slave processor having a first single master type bi-

directional communication interface unit and a first multi-master type bi-directional communication interface unit,

wherein ~~whose~~ the transmission speed of said first multi-master type bi-directional communication interface unit is ~~smaller~~ less than ~~that~~ the transmission speed of said first single master type bi-directional communication interface unit;

a master processor, which is defined ~~(defined~~ as a master to start communication with said ~~slave)~~slave, the master processor having a second single master type bi-directional communication interface unit and a second multi-master type bi-directional communication interface unit,

wherein the ~~whose~~ transmission speed of said second multi-master type bi-directional communication interface unit is ~~smaller~~less than ~~that~~ the transmission speed of said second single master type bi-directional communication interface unit;

a first transmission cable for connecting said first single master type bi-directional communication interface unit and said second single master type bi-directional communication interface unit; and

a second communication cable for connecting said first multi-master type bi-directional communication interface unit and said second ~~single~~ multi-master type bi-directional communication interface ~~unit;~~unit,

wherein said slave processor is equipped with a first command transmission means for transmitting a transmission request command to ~~ask~~ request said master processor to start ~~data~~ transmission of data from said first multi-master type bi-directional communication interface unit to said master processor via said second communication ~~cable;~~cable, and

wherein said master processor causes said second single master type bi-directional communication interface unit to start communication with said first single master bi-directional communication interface unit in response to said transmission

request command, which was received by said second multi-master type bi-directional communication interface unit, and sends said data to said slave processor via said first communication cable.

3. (currently amended): The multi-processor system of claim 2, wherein said first single master type bi-directional communication interface unit and said second single master type bi-directional communication interface unit are SPI (Serial ~~Communication~~ Peripheral Interface) units.

4. (currently amended): The multi-processor system of claim 2, wherein said first multi-master type bi-directional communication interface unit and said second multi-master type bi-directional communication interface unit are either ~~serial communication interface~~ SCI (Serial Communication Interface) units or IEEE1394 interface units.

5. (currently amended): The multi-processor system of claim 2,

wherein said master processor ~~has~~ includes a data communication means and an input means,

wherein said input means ~~which~~ connects to an input device and receives output data from said input device,

wherein said slave processor ~~contains~~ includes a program, which processes said output data received from said input device,

wherein said first command transmission means sends a first transmission request command which requests transmission of said output data received from said input device to said master processor via said first multi-master type bi-

directional communication interface unit in response to a request from said program, and

wherein said data communication means causes said second single master type bi-directional communication interface unit to start reception of said output data received from said input device in response to said first transmission request command when said second multi-master type bi-directional communication interface unit receives said first transmission request command.

6. (currently amended): The multi-processor system of claim 5,

wherein said master processor is equipped with a storage means which ~~is correspondent~~corresponds to said input device and stores a first input page to ~~contain~~ include said output data received from said input device,

wherein said slave processor is equipped with a storage means which contains a second input page ~~correspondent~~ which corresponds to said first input page,

wherein said first command transmission means sends said first transmission request command which contains a specification of said first input page, and

wherein said data communication means causes said second single master type bi-directional communication interface unit to start ~~to receive~~ receiving data from said first input page and to store said data received from said first input page in said second input page.

7. (currently amended): The multi-processor system of claim 2,

wherein said master processor ~~has~~ includes a data communication means and an output means,

wherein said output means ~~which~~ connects to an ~~input~~ output device and sends input data to said output device,

wherein said slave processor contains a program to calculate said input data,

wherein said first command transmission means transmits a second transmission request command which requests reception of said input data in response to a request from said program to said master processor via said first multi-master type bi-directional communication interface unit, and

wherein said data communication means causes said second single master type bi-directional communication interface unit to start data transmission to said output device in response to said second transmission request command when said second multi-master type bi-directional communication receives said second transmission request command.

8. (currently amended): The multi-processor system of claim 7,

wherein said slave processor has a storage means related to said output device and contains a first output page in which the input data of said output device is stored by said program,

wherein said first command transmission means transmits said second transmission request command which contains ~~the~~ a specification of said first output page,

wherein said data communication means causes said second single master type bi-directional communication interface unit to start transmission of said input data which is stored in said first output page indicated by the specification in said second transmission request command, and

wherein said master processor comprises a storage means which contains a second output page corresponding to said first output page and a data

communication means which stores, in said second output page, data which said second single master type bi-directional communication interface unit transmitted in response to said second transmission request command.

9. (currently amended): The multi-processor system of claim 2,

wherein said master processor contains a first program,

wherein said slave processor contains a second program which cooperates with said first program, said first command transmission means transmits a first transmission request command which requests to transmit output data of said first program and a second transmission request command which requests to receive output data of said second program in response to a request from said second program to said master processor via said master processor, and

wherein said data communication means causes said second single master type bi-directional communication interface unit to start transmission of output data of said first program to said second multi-master type bi-directional communication interface unit in response to said first transmission request command when said second multi-master type bi-directional communication interface unit receives said first transmission request command and causes said second multi-master type bi-directional communication interface unit to start reception of the output data of said second program to said first single master type bi-directional communication interface unit in response to said second transmission request command when said second multi-master type bi-directional communication interface unit receives said second transmission request command.

10. (currently amended): The multi-processor system of claim 2,

wherein a third communication cable is provided to connect said first multi-master type bi-directional communication interface unit and said second multi-master type bi-directional communication interface unit,

wherein said master processor is equipped with a second command transmission means which transmits a command to said slave processor from said second multi-master type bi-directional communication interface unit via said third communication cable,

wherein this second command transmission means transmits a confirmation message to said slave processor via said second communication cable from said second multi-master type bi-directional communication interface unit when said second multi-master type bi-directional communication interface unit receives said transmission request command via said second communication cable, and

wherein said first command transmission means transmits a confirmation message to said master processor via said third communication cable when said second multi-master type bi-directional communication interface unit receives said transmission command via said third communication cable.

11. (original): The multi-processor system of claim 2, wherein said first multi-master type bi-directional communication interface unit is provided inside or outside of said slave processor and said second multi-master type bi-directional communication interface unit is provided inside or outside of said master processor.